Homework 8

Solutions

- 1. Fairness
 - (C) A fair implementation might cause either and underflow or an overflow. Fairness simply requires that the nondeterministic choice eventually selects each action. Since there is no time-bound on how long it might take before the nodeterministic choice selects a particular action, it is possible to either overflow or underflow. The same can be said of an unfair implementation since in that case, there is no requirement to choose a particular alternative eventually.
 - (b) A fair implementation requires that eventually every alternative is selected. Thus, eventually the go := false line will be executed meaning the incrementing of n will eventually stop.

Under an unfair implementation there is no requirement to select a particular option and so the code might increment n forever.

- (C) Simpler on a single-processor since you don't need to synchronize the multiple processors. "Everything is easier on a single-processor language implementation." —Adam Barth
- 2. Actor computing
 - (a) A sequence number can be added to each task. When *B* first receives a task, it can check the sequence number. If this is not the first task, or the next one to be processed, then *B* should store the task and process it later in order.
 - (b) One protocol, similar to TCP, is for B to acknowledge each received message (by sequence number). To avoid flooding the communication mechanism, A can send a few messages, then wait for acknowledgements to arrive before proceeding with additional messages. If A receives acknowledgements for several messages with sequence numbers greater than n, then A can suspect that message n is delayed and resend it.
 - (C) The *I'm done* message should have a sequence number too.

		Synchronous		Asynchronous	
3 Message Passing		Ordered	Unordered	Ordered	Unordered
	Buffered			TCP	Actor/Java
	Unbuffered	CML			UDP

- (a) Buffered synchronous makes no sense because you don't need to buffer things if everything is synched up.
- (b) Synchronous unordered makes no sense because if you are synched you cannot receive messages out of order.
- (C) Asynchronous unbuffered message-passing cannot be ordered so the ordered asynched unbuffered version makes no sense.

- 4. CML Thread Implementation
 - (a) The program outputs numbers from 0-100 in two columns, one number in each row. Even numbers are printed in the first column and odd numbers in the second. The number are produced by two threads "skipby(0,2)" and "skipby(1,2)", which yield to each other at psuedorandom intervals.

- (C) Yes, because we have non-preemptive scheduling and the threads yield to each other at pseudo-random (i.e. deterministic) intervals.
- (d) Programmers can now determine exactly when control leaves the current thread, so there is less chance of unexpected interleavings that can lead to race conditions.

(C) Since the two threads can occur in any order with respect to each other, you get two different constraint graphs, one for thread one and the other for thread 2.

read x	\rightarrow	load $x \rightarrow$	use x	\rightarrow	assign a	\rightarrow	store a	\rightarrow	write a
					.↓				
					assign y				
					\downarrow				
					store y				
					\downarrow				
					write y				
1		1 1					, 1		• • •
read y	\rightarrow	$\text{load } y \rightarrow$	use y	\rightarrow	assign b	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	$\text{load } y \rightarrow$	use y	\rightarrow	assign b \downarrow	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	load y \rightarrow	use y	\rightarrow	assign b ↓ assign x	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	$load \; y \rightarrow$	use y	\rightarrow	\downarrow	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	load y \rightarrow	use y	\rightarrow	\downarrow	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	load y \rightarrow	use y	\rightarrow	$assign x \downarrow$	\rightarrow	store b	\rightarrow	write b
read y	\rightarrow	load y \rightarrow	use y	\rightarrow	$assign x \downarrow$	\rightarrow	store b	\rightarrow	write b

(b) Here for the prescient stores, the store need not wait for its assign.

 $\begin{array}{rrr} {\rm read}\; x \; \rightarrow \; {\rm load}\; x \rightarrow \; {\rm use}\; x \; \rightarrow \; {\rm assign}\; a \qquad {\rm store}\; a \; \rightarrow \; {\rm write}\; a \\ & \downarrow \\ {\rm assign}\; y \\ & {\rm store}\; y \\ & \downarrow \\ {\rm write}\; y \end{array}$