Computer Science Comprehensive Examination
Computer Architecture
[60 points]

This examination is open book. Please do all of your work on these sheets. Do not do your work in a blue book.

Number: _____

Problem	*Max Score*	*Your Score*
1	20	
2	20	
3	20	
TOTAL	60	

Problem 1: Short Answer [20 points]

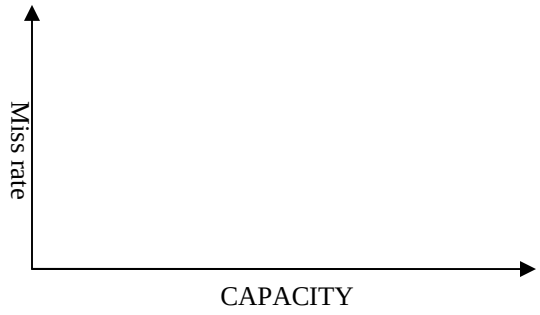
A. [7 points] Assume a pipelined processor with N pipeline stages. As we increase N, briefly explain that happens to the following (increase/decrease + 1 sentence reasoning)

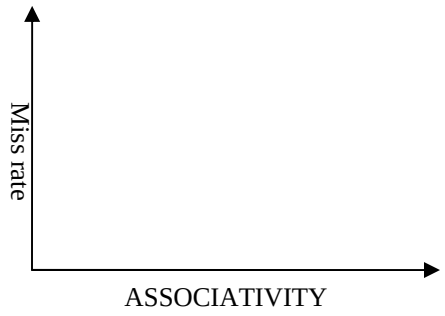
- Clock cycle time:

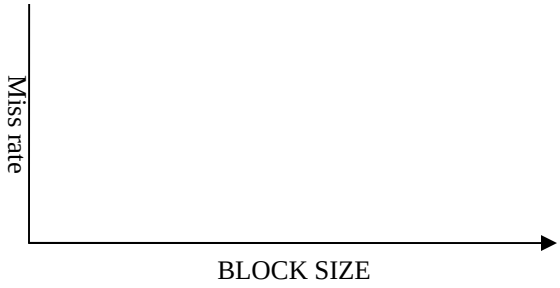
- Cycles per instruction:

Considering clock cycle time only, is there a limit or point of diminishing returns for the number of pipeline stages in a processor? Why?

B. [7 points] Assume a first level data cache with capacity (C), associativity (A), and block size (B). Draw the expected effect on hit rate as C, A, and B increase respectively. In each case, we vary one of the three parameters, while the other two are kept constant. Mark one or two interesting points on the graphs with 3-4 words to provide some reasoning.







C. [6 points] What does the following MIPS code do when it is invoked with the register $a0 containing the value 0x2000? What is the instruction cache miss rate? What is the data cache miss rate? Assume the caches are initially empty, allocate lines on both load and store misses, and have a 16 byte line size.

```
0x1000:                move $t0, $a0
0x1004:                addi $t1, $t0, 4000
0x1008:      loop:     sw   $t0, 0($t0)
0x100C:                addi $t0, $t0, 4
0x1010:                slt  $t2, $t0, $t1
0x1014:                bne  $t2, $zero, loop
0x1018:      exit:
```

Problem 2: Instruction-Set Architecture Design [20 Points]

Your task is to redesign the way branches work in the MIPS ISA to create a new architecture called MIPS-new. You decide to add branches with arbitrary compares, which are called complex branches. You are given the following information about MIPS and MIPS-new:

Instruction mix on MIPS:

Instruction type	*Frequency*
compares	23%
ALU ops (not compares)	20%
loads/stores	30%
conditional branches	25%
jumps	2%

Frequency of branch compares on MIPS-new:

Branch type	*Frequency*
NE/EQ compare to nonzero	10%
NE/EQ compare to zero	5%
LT/LE compare to nonzero	30%
GT/GE compare to zero	5%
LT/LE compare to nonzero	45%
GT/GE compare to zero	5%

A. [9 points] Using the information given above, what is the ratio of instruction count (IC) of MIPS to MIPS-new. You may assume that the compiler transforms a compare-branch instruction pair into a complex branch whenever possible.

B. [9 points] Complex branches in MIPS-new force you to move the branch decision point from the ID stage to the EX stage. To maintain compatibility with MIPS, you decide to use delayed branching for the first cycle of branch delay and to predict taken for any subsequent cycles of branch delay. Assume that the target PC is calculated in the ID stage. If the delay slot is usefully filled 50% of the time and branches are taken 70% of the time, what is the ratio of CPIs of MIPS to MIPS-new? Assume that noops do not count as instructions and all instructions except branches and jumps have a CPI of 1.0.

C. [2 points] Which architecture is better? Why?

Problem 3: Memory Hierarchy Design [20 Points]

You have a computer with two levels of cache memory and the following specifications:

- Processor: 2GHz, 64-bit RISC CPU
- On-chip L1 caches
  - split instruction & data cache, blocking, single-ported
  - write-through & non-write allocate
  - 1 CPU cycle access time (i.e. hits do not stall the processor)
  - Block size = 32 bytes
- Off-chip L2 cache
  - unified single-ported cache, blocking
  - write-back
  - 10 CPU cycles access time (L1 miss penalty) for both reads and writes
  - Block size = 32 bytes
- Main memory:
  - Bus: 64-bit data transfers at 400 MHz
  - Latency: 15+5+5+5 CPU cycles access time for 32 bytes (L2 miss penalty – includes latency of both DRAM and memory bus)

A. What is the:

- Peak L1 data cache bandwidth available to CPU (assuming 0% L1 misses)?
- Peak L2 cache bandwidth available to L1 cache (assuming 0% L2 misses)?
- Main memory bandwidth available to L2 cache?

Report the bandwidths in Gbytes/sec, i.e. 2^{30} bytes/sec.

B. You are given the following L1 cache statistics for a program executing on this system

Metrics	Access Type: Total	Instrn	Data	Loads	Stores
Accesses	10000000	7362210	2637790	1870945	766845
Misses	52206	8466	43740	36764	6976

Words Read From Lower-levels	180920 (i.e. 45230 cache lines)
Words Written-back to Lower-levels	766845
Total Traffic	947765

How long does an average instruction take to execute (in ns), assuming 1 clock cycle per instruction in the absence of memory hierarchy stalls, no write buffering at the L1 cache level, and 0% L2 miss rate? Ignore register dependencies between instructions.